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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,789	01/15/2002	Jin-Young Park	8836-147 (IB11125-US)	5610

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/047,789	Applicant(s) PARK, JIN-YOUNG	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because Figs 4A, 4B and 5 are cited in the specification but are missing from the file. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because it fails to comply with the proper language and format for an abstract of the disclosure.

The terms "comprising", "disclosed" and "comprises" cited on lines 1, 2 and 8 should be deleted. The form and legal phraseology often used in patent claims, such as "comprising, comprises " should be avoided. The language should be clear and concise and it should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 1-10 are objected to because of the following informalities:

Claim 1, "a defect, if any, of the memory chip" should be changed to "a defect of the memory chip".

Claim 10 recites the limitation "data combinations that two random memory cells having mutually different addresses have", which appears to be grammatically incomprehensible due to the use of terms "having" and "have". Appropriate correction is required.

Claims 2-9 are also objected due to their dependency from a main objected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Treuer (US 6694461) FILED: July 26, 1999.

Regarding independent Claims 1 and 11, Treuer discloses an apparatus and method for BIST (built-in self-test) circuit, including a Test Mode Controller (250) and Test Collars (231-235) as shown in (FIG. 2), comprising:

A controller (250) for controlling a self-testing operation of a memory chip (200) having memories (221-225) embedded in an integrated circuit (FIG. 2).

An address generator (WRITE ADDR GENERATOR, FIGS. 3 and 4) for generating pseudo-random address patterns using primitive polynomial-based pseudo-random bit-streams, under the control of the controller (250), also, see abstract.

A data generator (DATA GEN, FIGS. 3 and 5) for producing test data associated with data backgrounds of the address bits by utilizing the address values to generate data values (FIG. 8, step 802, also see abstract), which is under the control of the controller (250).

A comparator (DATA COMP, FIGS. 3 and 6) for comparing the test data, such as expected data values (FIG. 8, 804) which are generally the same as the data stored in memory, with the memory data output (READ DATA-OUT) from the memory chip to detect, a defect, if any, of the memory chip.

Regarding Claims 2, 10 and 12, Treuer discloses March algorithms, which read and write data in an up direction (incrementing address values) or in a down direction, such as a binary up-down counters or LFSRs registers for counting up or down the data backgrounds of the address bits in a single-order for generating an address. (Col. 1, lines 35-45 and Col. 11, lines 5-15).

Regarding Claims 3, 4, 7-9 and 13, Treuer discloses address generator (WRITE ADDR GENERATOR, FIGS. 3 and 4) including a plurality of linear feedback shift registers (LFSRs) (410, 420, FIG. 4) connected to each other for producing the pseudo-random address patterns, where the down-direction shift-register 420 is used as the

down-direction address source and up-direction shift register 410 is used as the up-direction address source and where controller (250) controls the plurality of LFSRs (410, 420). The plurality of LFSRs further comprises a counter for counting the address bits to produce the pseudo-random address patterns, where the shift register 410 is replaced by a binary up-only counter (col. 11, lines 5-10).

Regarding Claim 5, 6 and 14, Treuer discloses a 4-bit version of a data generator (FIG. 5) comprising, a first multiplexer coupled to the address bits (TADR0-TADR3) and a ground voltage as input values and selecting one of the input values in response to a first control signal (USE-ADDR, EVEN or ODD) from the BIST controller (250) and a second multiplexer for selecting the test data bits (TDATA0-TDATA3) from the output of the first multiplexer, in response to a second control (POLARITY) signal from the controller, wherein the first control signal (USE-ADDR, EVEN or ODD) comprises a current data background of the address bits (TADR0-TADR3) and the second control (POLARITY) signal comprises a complemented data background of the address bits (TEXPECT0-TEXPECT3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 5 May 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100